Solid State Relays Overview And Applications

AN3000

CONTENTS

1. INTRODUCTIION

The SSR that NEC has started marketing uses a photocoupler system with a MOS FET, explained in the following, as an output switch and a combination of an Emitter and Photo Detector to drive the switch.

NEC's SSR is named a "OCMOS FET (Opto-Coupled MOS FET)" as the input and output are isolated with a photocoupler and the MOS FET switch is used as an output switch.

The OCMOS FET using a photo Detector to drive the MOS FET is a new type of SSR developed recently and being commercialized.

An OCMOS FET operates this way: A control signal applied to the OCMOS FET input terminals triggers the output switch of the OCMOS FET, which, in turn, opens or closes the output terminals.

A normally-off type (which is functionally the same as a "make contact" mechanical relay) leaves the output terminals open, if there is no input signal, and short-circuits the output terminals if an input signal above the threshold level is applied. Conversely, a normally-on type (which is functionally the same as a "break contact" mechanical relay) keeps the output terminals short-circuited, if there is no input signal, and opens the output terminals by an input signal.

2. FEATURES, STRUCTURES, COMPOSITION AND THEORY OF OPERATION

2.1 FEATURES

The general features of OCMOS FET as follows:

1) High sensitivity and low driving power. Can be driven directly by a TTL or CMOS.
2) Can switch low to high-voltage level signals or an AC/DC load current at a low power level.
3) Extremely low offset voltage (in the on-state) and very small leakage current (in the off-state). Applicable even to low-level signals.
4) dv/dt insensitive, No possibility of malfunction caused by noise signals due to abrupt startup. No thermal runaway, as seen bipolar elements.
5) Use of bidirectional MOS FET support DC and AC switching.
6) A compact DIP/SOP package which can be mounted like other electronic components.

2.2 STRUCTURES

Compared with a mechanical relay, the input and output control sections, made up of the LED and PVD in the OCMOS FET, correspond to the coil in the mechanical relay. They isolate the input from output and generate an output control signal on receipt of an input signal.

The MOS FET in the OCMOS FET corresponds to the contact in the mechanical relay, opening and closing the load circuit.

Figure 1 shows the OCMOS FET structure. Figure 2 shows the sectional view. The semiconductor chip, a subcomponent of the OCMOS FET is mounted at a required position on the metal support, called a lead frame, also serving as a terminal, using conducting paste. (The procedure is called chip mounting.)

Next, the chip electrodes are connected to a fine gold wire to the lead, which becomes a terminal. (The procedure is called wire bonding.) Then as regards face-to-face type, the LED and PVD are covered with transparent silicone rubber to form an optical path. This is put into a furnace for hardening and then molded with epoxy resin.

There is more than one kind of structure that links LED and PVD (called a photocoupler structure). Table 1 shows an example of the structure type and Table 2 compares the different structures. (NEC's OCMOS FET series are face-to-face type and double mold type.)

Figure 1. OCMOS FET STRUCTURE

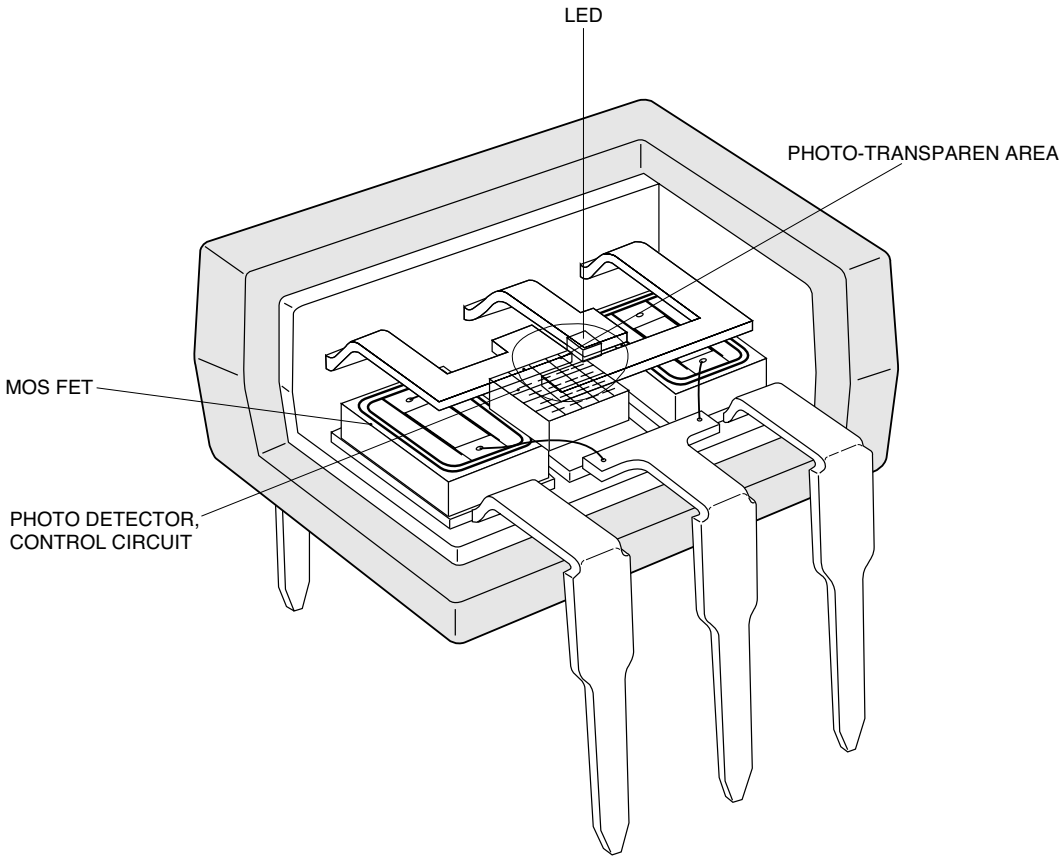


Figure 2. SECTIONAL VIEW

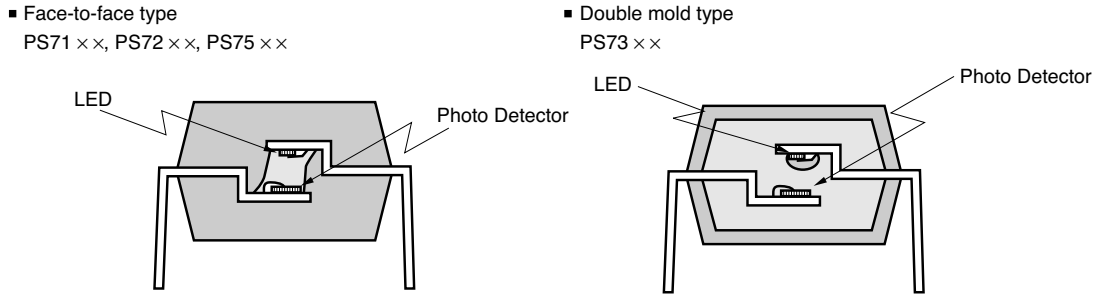


Table 1. Photocoupler Structure

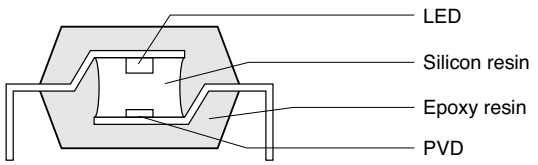
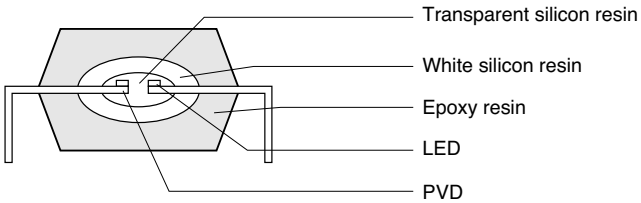
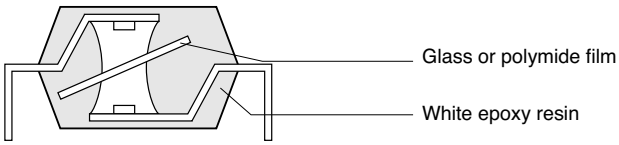
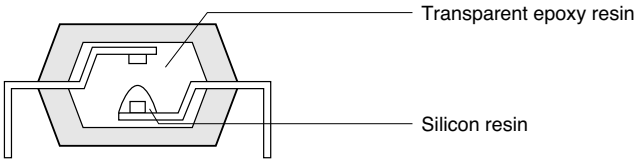
No.	Structure type	Structure
1	Face-to-face format	
2	Coplanar format	
3	Insulated format	
4	Double mold format	

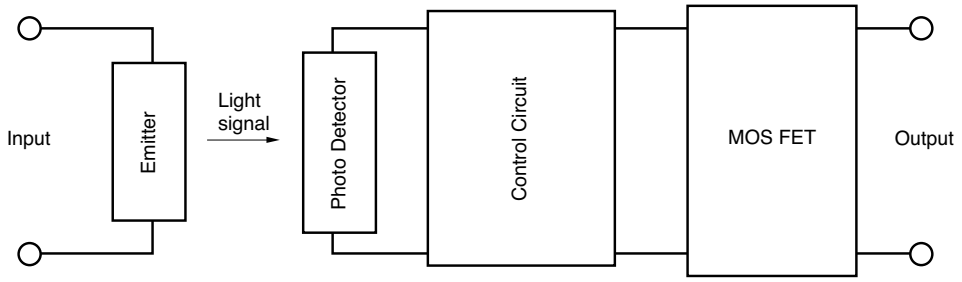
Table 2. Photocoupler Structure (Internal view)

Structure type	Optical Transmission		Insulation	Moisture Resistance	Productivity
	Efficiency	Stability			
Face-to-face format	Good	Fair	Fair	Fair	Fair
Coplanar format	Fair	Good	Good	Fair	Excellent
Insulated format	Excellent	Fair	Good	Fair	Poor
Double mold format	Fair	Good	Excellent	Good	Fair

2.3 COMPOSITION

As shown in Figure 3, the NEC OCMOS FET consists of an Emitter, Photo Detector, Control Circuit, and the MOS FET.

Figure 3. OCMOS FET COMPOSITION



Emitter: LED Photo Detector: PVD (Photo Voltaic Diode)

2.4 THEORY OF OPERATION

Normally-off type. Theory of operation as follows.

When an input signal current flows across the input terminals, the LED emits light. Some of the light is shot directly into the PVD via the transparent silicon layer, while the rest of the light reaches the PVD after being reflected from the transparent silicon boundary surface. On receiving the light, the PVD generates a current corresponding to the amount of incident radiation received.

The current passes through the control section to charge the MOS FET gate capacity, raising the gate voltage. When the gate voltage reaches a certain voltage value, current flows between the MOS FET drain and source. Since the drain and source are connected to the output terminals, the external load circuit across the output terminals is closed.

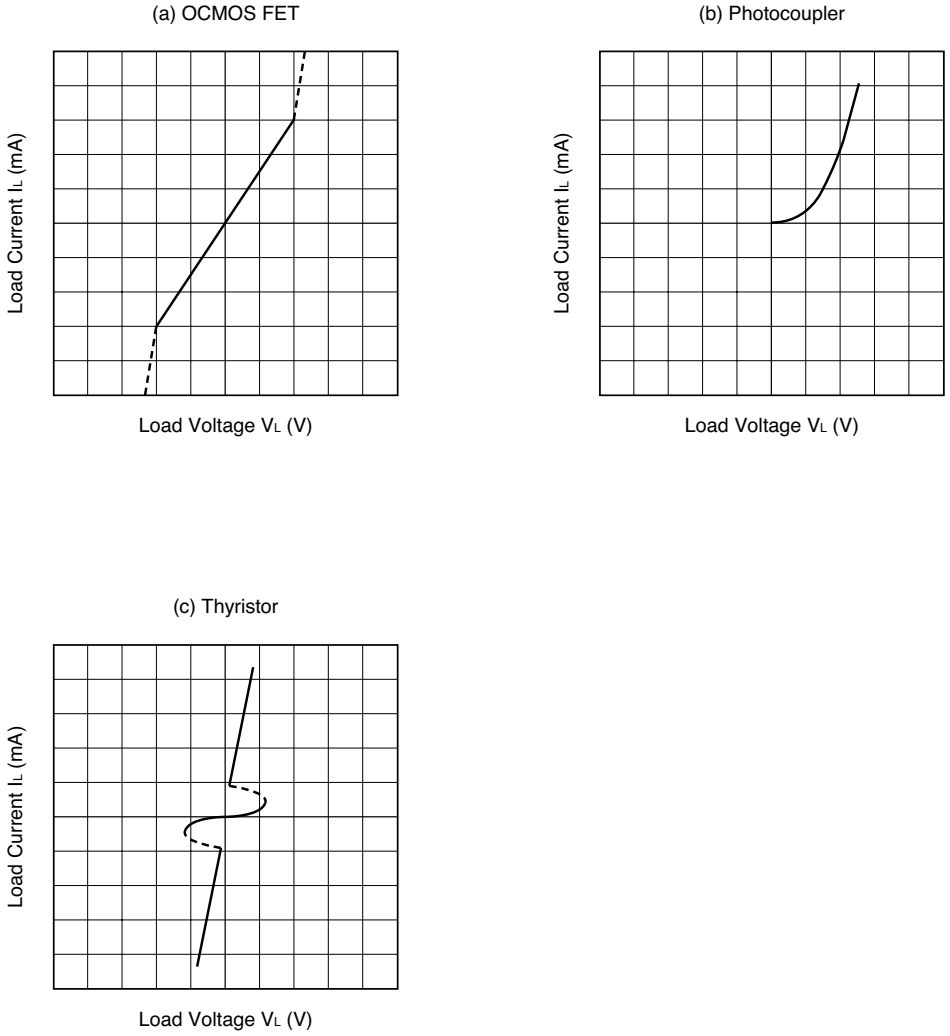
When the input signal current is disconnected, the LED stops emission and the PVD voltage drops. In this condition, the charges stored in the MOS FET gate are not released quickly, instead the FET remains conductive. If the control circuit is operated to cause the MOS FET gate charges to be released quickly, the MOS FET gate voltage will be dropped. If the voltage drops to a certain level, the MOS FET drain and source will be isolated again.

3. MAINLY CHARACTERISTICS

3.1 OFFSET VOLTAGE

Figure 4 shows LOAD CURRENT (I_L)-LOAD VOLTAGE (V_L) characteristic for the MOS FET. When V_L is low, the current changes, as in a DC in a DC resistor. That is, there is no offset voltage.

Figure 4. Comparing OCMOS FET with a Photocoupler and Thyristor



3.2 TEMPERATURE CHARACTERISTICS

3.2.1 TURN-ON TIME CHARACTERISTICS

Figure 5 shows the NORMALIZED TURN-ON TIME vs. AMBIENT TEMPERATURE and the TURN-ON TIME DISTRIBUTION of a normally-off type OCMOS FET. (Such as the PS7112, PS7113, PS7122, PS7141, PS7142 and PS7160 OCMOS FET.)

3.2.2 TURN-OFF TIME CHARACTERISTICS

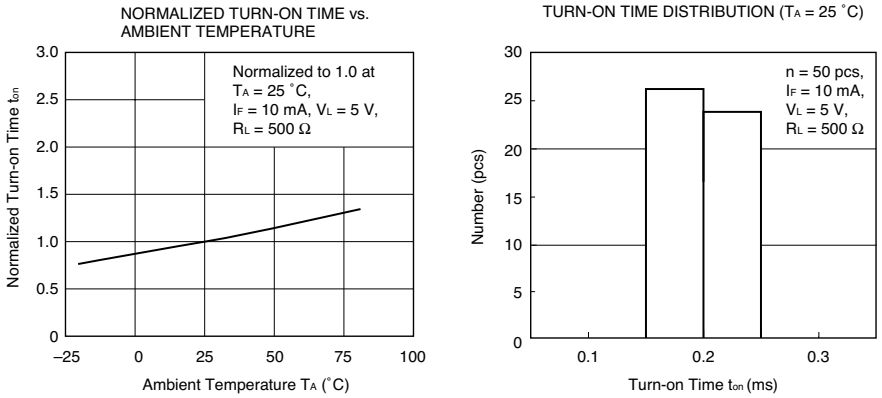
Figure 6 shows the NORMALIZED TURN-OFF TIME vs. AMBIENT TEMPERATURE and the TURN-OFF TIME DISTRIBUTION of a normally-off type OCMOS FET. (Such as the PS7112, PS7113, PS7122, PS7141, PS7142 and PS7160 OCMOS FET.)

3.2.3 ON-STATE RESISTANCE CHARACTERISTICS

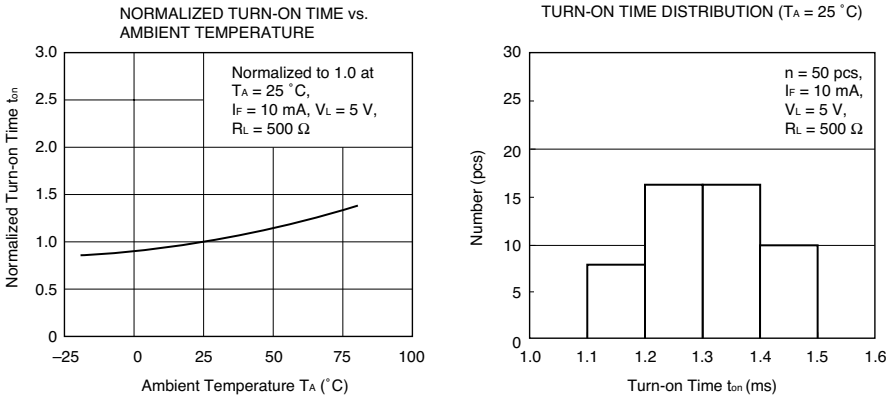
Figure 7 shows the NORMALIZED ON-STATE RESISTANCE vs. AMBIENT TEMPERATURE and the ON-STATE RESISTANCE DISTRIBUTION of a normally-off type OCMOS FET. (Such as the PS7112, PS7113, PS7122, PS7141, PS7142 and PS7160 OCMOS FET.)

Figure 5. NORMALIZED TURN-ON TIME vs. AMBIENT TEMPERATURE AND TURN-ON TIME DISTRIBUTION (1/2)

1) PS7112-1A, PS7112L-1A



2) PS7113-1A, -2A, PS7113L-1A, -2A



3) PS7122-1A, -2A, PS7122L-1A, -2A

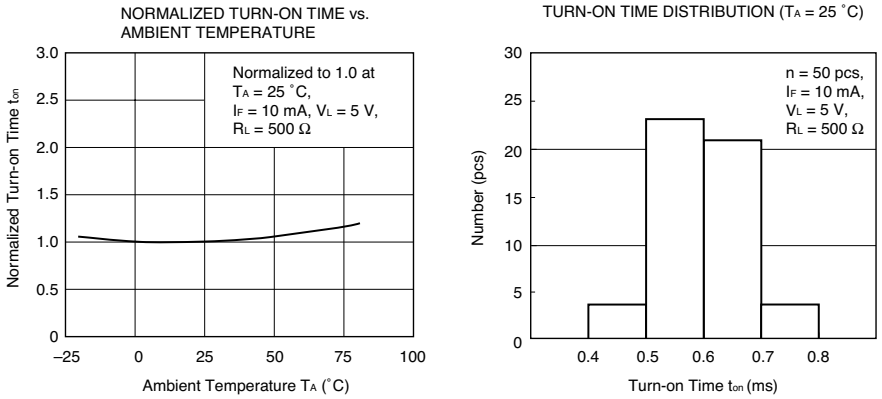
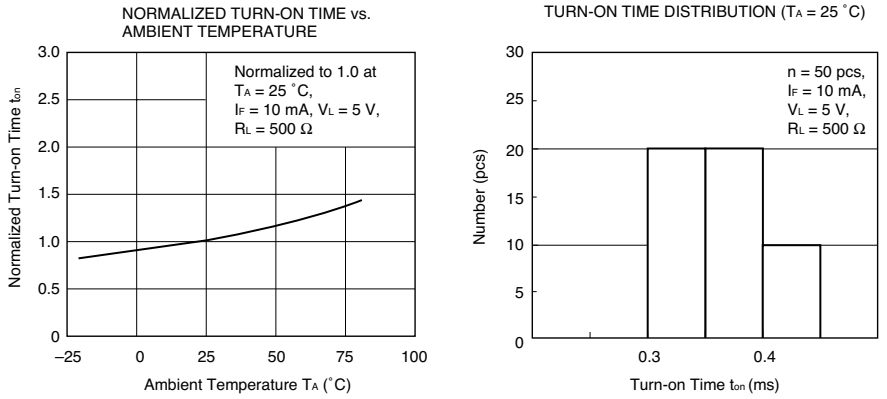
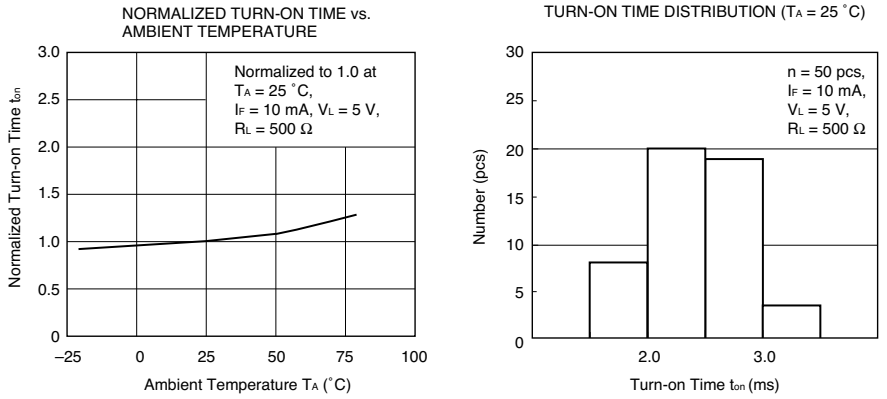


Figure 5. NORMALIZED TURN-ON TIME vs. AMBIENT TEMPERATURE AND TURN-ON TIME DISTRIBUTION (2/2)

4) PS7141-1A, PS7141L-1A



5) PS7142-1A, PS7142L-1A



6) PS7160-1A, PS7160L-1A

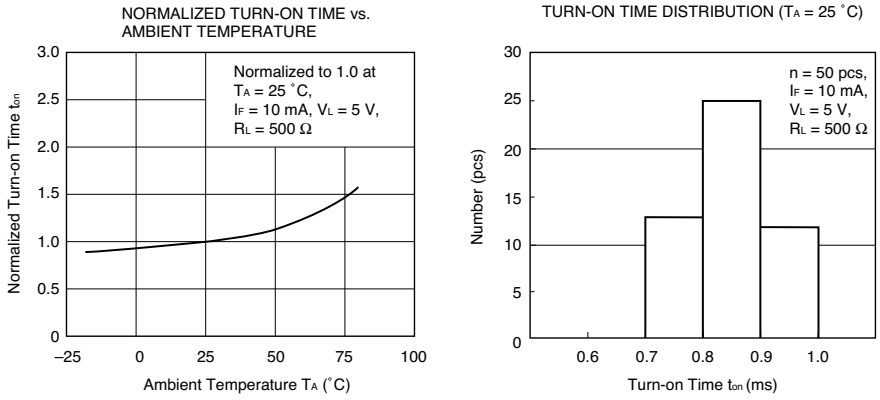
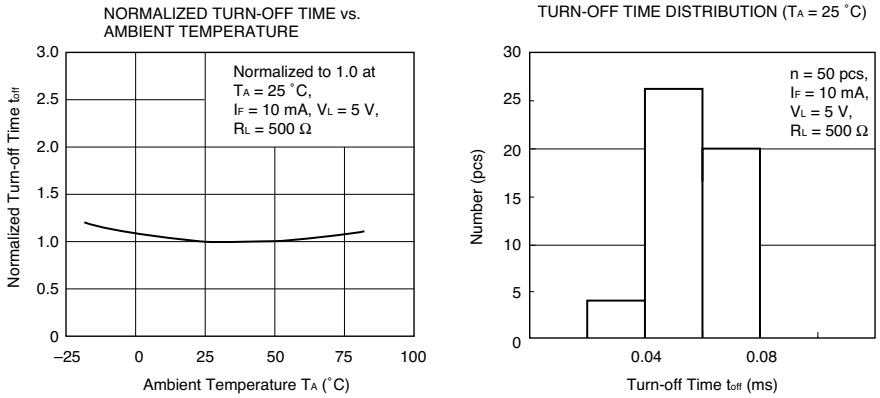
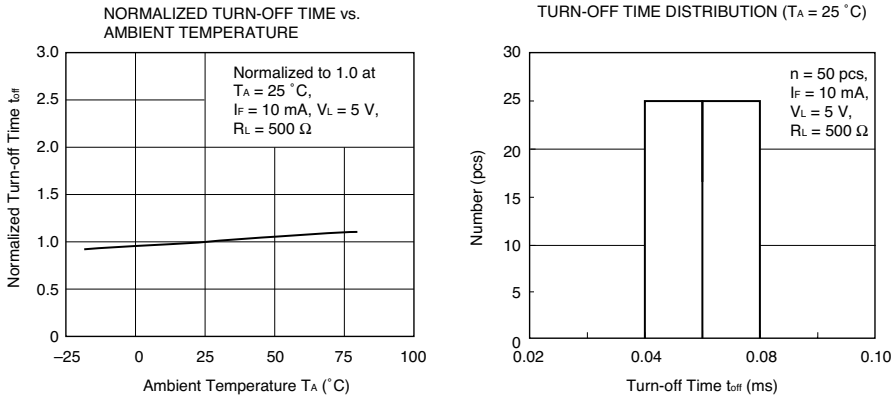


Figure 6. NORMALIZED TURN-OFF TIME vs. AMBIENT TEMPERATURE AND TURN-OFF TIME DISTRIBUTION (1/2)

1) PS7112-1A, PS7112L-1A



2) PS7113-1A, -2A, PS7113L-1A, -2A



3) PS7122-1A, -2A, PS7122L-1A, -2A

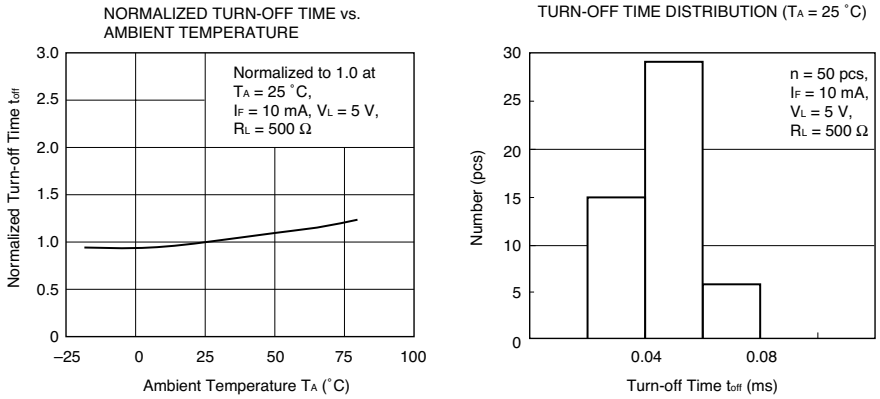
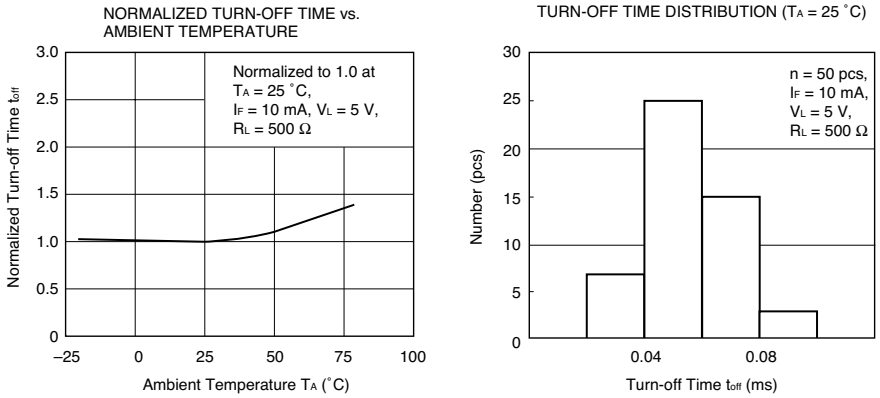
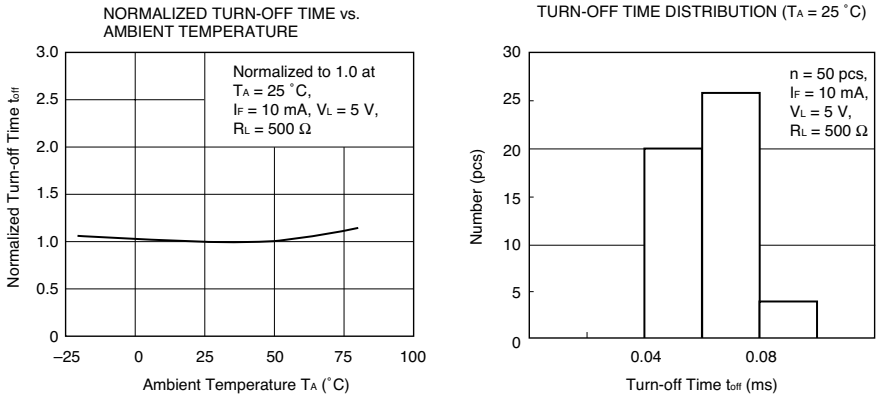


Figure 6. NORMALIZED TURN-OFF TIME vs. AMBIENT TEMPERATURE AND TURN-OFF TIME DISTRIBUTION (2/2)

4) PS7141-1A, PS7141L-1A



5) PS7142-1A, PS7142L-1A



6) PS7160-1A, PS7160L-1A

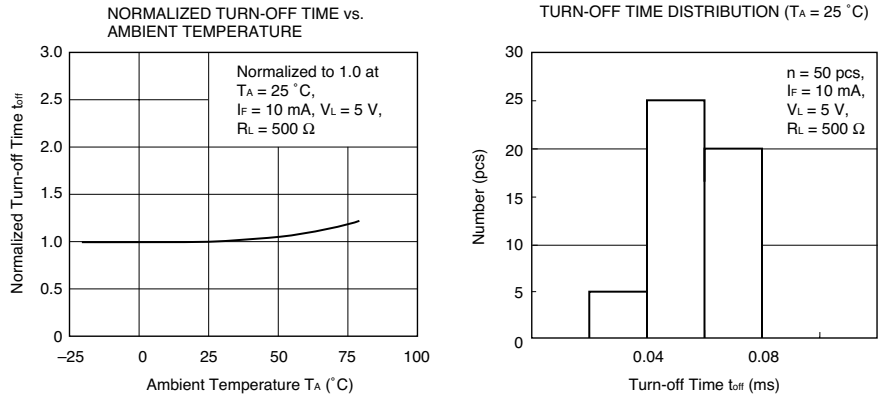
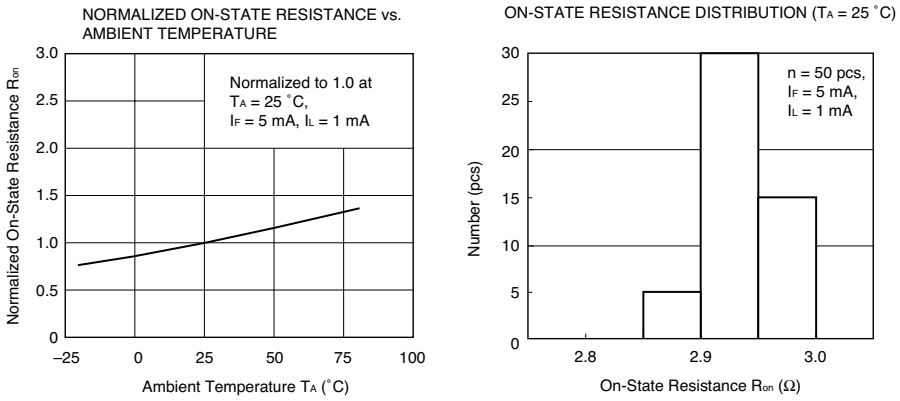
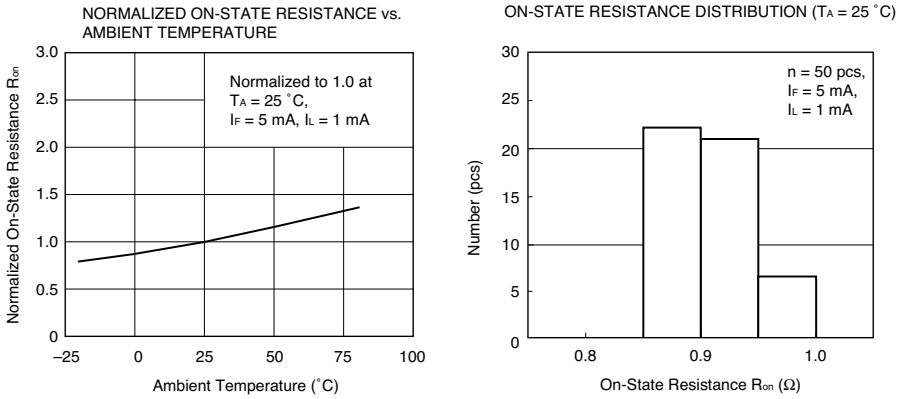


Figure 7. NORMALIZED ON-STATE RESISTANCE vs. AMBIENT TEMPERATURE AND TURN-ON TIME DISTRIBUTION (1/2)

1) PS7112-1A, PS7112L-1A



2) PS7113-1A, -2A, PS7113L-1A, -2A



3) PS7122-1A, 2A, PS7122L-1A, -2A

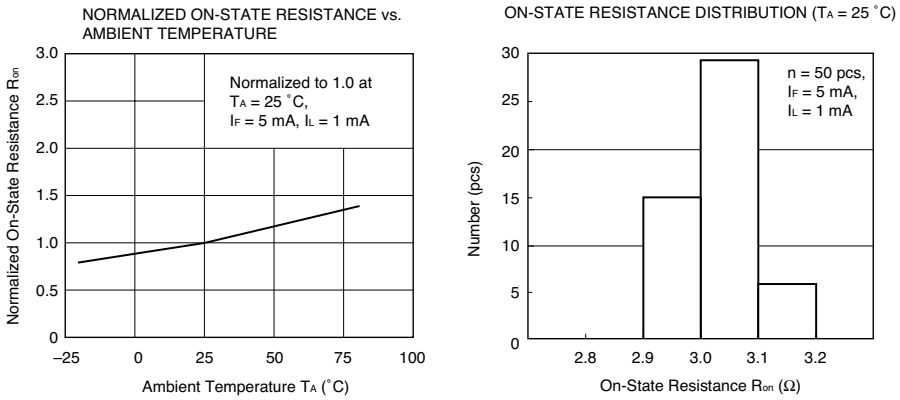
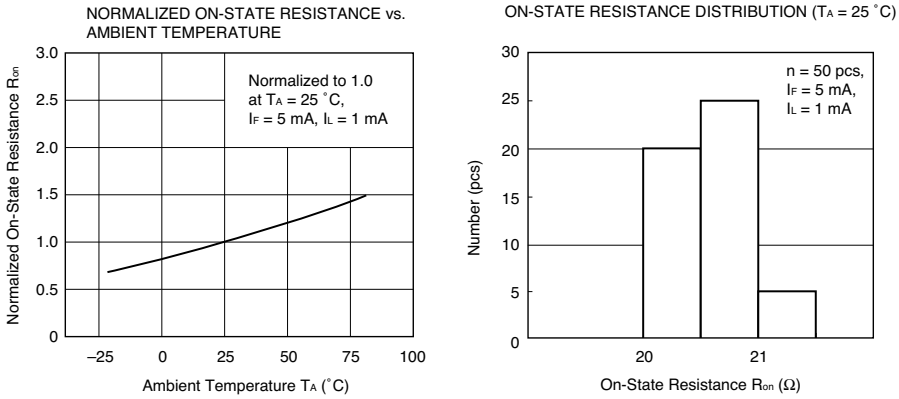
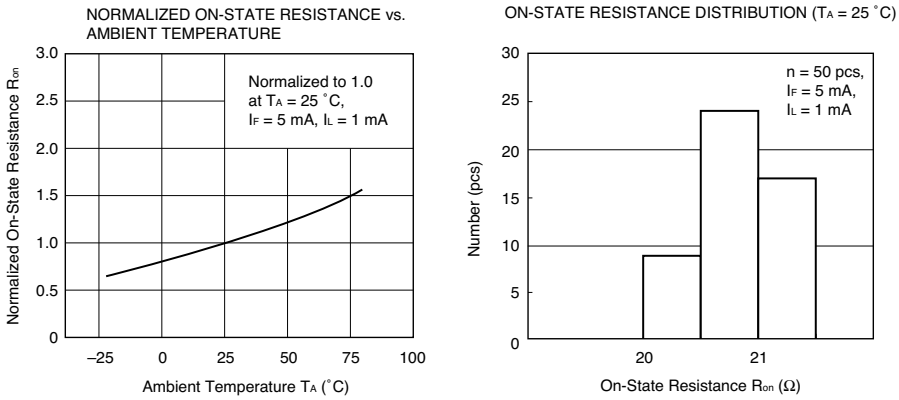


Figure 7. NORMALIZED ON-STATE RESISTANCE vs. AMBIENT TEMPERATURE AND TURN-ON TIME DISTRIBUTION (2/2)

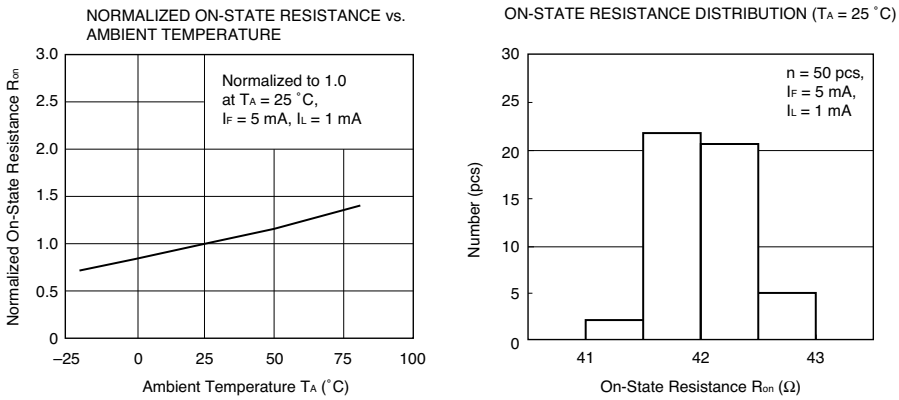
4) PS7141-1A, PS7141L-1A



5) PS7142-1A, PS7142L-1A



6) PS7160-1A, PS7160L-1A



4. CHARACTERISTICS VALUES AND MEASURING CHARACTERISTIC VALUES

4.1 CHARACTERISTICS VALUES

Table 3. OCMOS FET CHARACTERISTICS VALUES

Classification	Symbol	Item	Measuring Circuit Number
LED	V_F	Forward voltage	1
	I_F	Forward current (DC)	1
	V_R	Reverse voltage	2
	I_R	Reverse current	2
	C_t	Input capacitance	3
	P_D	Power dissipation	?
MOS FET	V_L	Breakdown voltage	4
	I_{Loff}	Off-state leakage current	5
	R_{on}	On-state resistence	6
	C_O	Output capacitance	7
Coupled	R_{I-O}	Isolation resistence	8
	BV	Isolation voltage (AC voltage for 1 minute at T_A = 25 °C, RH = 60 % between input and output).	9
	C_{I-O}	Isolation capacitance	10
	t_{on}	turn-on time	11
	t_{off}	turn-off time	11
	SOA	Safe operation area (DC)	?
	SOA	Safe operation area (pulse)	?

4.2 MEASURING CHARACTERISTIC VALUES

Table 4. Measuring OCMOS FET Characteristic Values (1/3)

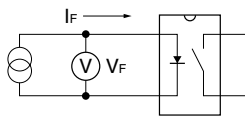
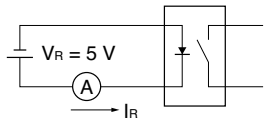
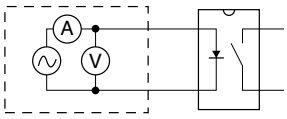
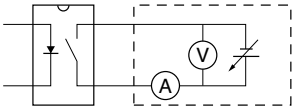
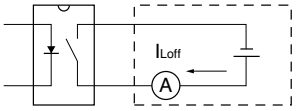
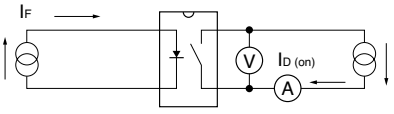
Measuring Circuit Number	Characteristic Value	Measuring Method and Conditions	Measuring Circuit
1	Forward voltage (V_F)	Let a required current flow across control input terminals and measure the voltage. I_F = 10 (mA)	(Control input side) 
2	Reverse current (I_R)	Apply a voltage across control input terminals in a direction opposite to normal and measure the current. V_R = 5 (V)	
3	Input capacitance (C_t)	Connect an LCR meter to control input terminals and measure the electrostatic capacitance. V = 0 (V), f = 1 (MHz)	 LCR meter, etc.
4	Breakdown voltage (V_L)	Step up a voltage slowly across switching terminals and measure the voltage at which a required current begins flowing. $I_{D(BD)}$ = (to be defined)	 Semiconductor multimeter, etc.
5	Off state leakage current (I_{Loff})	Apply a required voltage across switching terminals and measure the current. $V_{D(BD)}$ = Rated voltage (V)	 Semiconductor multimeter, etc.
6	On-state resistance (R_{on})	Let a required current flow across control input terminals, close the switch, and measure the resistance across the terminals. I_F = 5 (mA) I_L = 1 (mA)	 $R_{on} = \frac{V}{I_L}$

Table 4. Measuring OCMOS FET Characteristic Values (2/3)

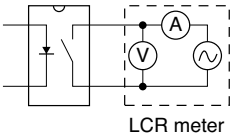
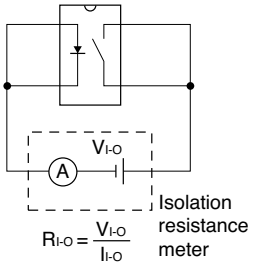
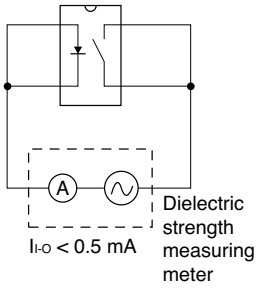
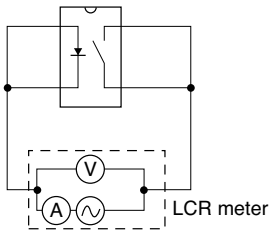
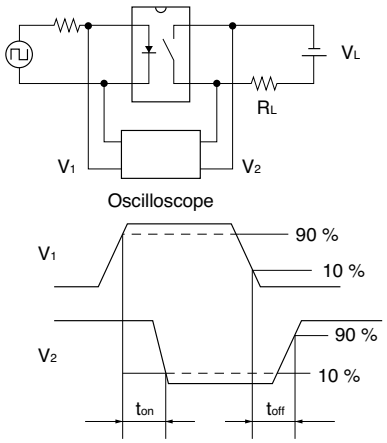
Measuring Circuit Number	Characteristic Value	Measuring Method and Conditions	Measuring Circuit
7	Output capacitance (C_O)	Connect an LCR meter across switching terminals, apply a required DC overlapping voltage, and measure the electrostatic capacitance. V = 0 (V), f = 1 (MHz)	
8	Isolation resistance (R_{I-O})	Connect an Isolation resistance meter between control input terminals and switching terminals, apply a required voltage, and measure the resistance. V_{I-O} = 1 (kV)	
9	Isolation voltage (BV)	AC voltage for 1 minute at T_A = 25 °C, RH = 60 % between input and output.	
10	Isolation capacitance (C_{I-O})	Connect an LCR meter between control input terminals and switching terminals and measure the electrostatic capacitance. V = 0 (V), f = 1 (MHz)	

Table 4. Measuring OCMOS FET Characteristic Values (3/3)

Measuring Circuit Number	Characteristic Value	Measuring Method and Conditions	Measuring Circuit
11	turn-on time (t_{on}) turn-off time (t_{off})	Apply a rectangular wave AC voltage, to cause a required current to flow across control input terminals, and connect a load across switching terminals that satisfies a required current and voltage. Measure the waveforms for the voltages across control input terminals and across switching terminals, using a time measuring instrument like an oscilloscope, as shown at the right. I_F = 10 (mA) R_L, V_L } (to be defined)	

5. APPLICATIONS

With the above features and characteristics, this OCMOS FET is suitable for the following uses: And Table 5 shows OCMOS FET LINE-UP and application.

5.1 COMMUNICATION LINES

In communication lines, relative by high voltages are applied, including office power, call signals, and test signals. Moreover, lightning surge induced in a line may unavoidably leak out to the equipment through a protective circuit.

Accordingly, a high breakdown voltage is required for the communication equipment connected to the communication lines. A photocoupler SSR is suitable to prevent relay drive current from flowing into the lines.

Furthermore, since the polarity of the telephone line is reversed in the exchange operation, the relay contact inserted in the line should have a bidirectional characteristic.

The OCMOS FET satisfies these conditions and is suitable for these applications. The applicable equipment includes an office exchange, PBX, key telephone, telephone, and facsimile.

Figure 8 and Figure 9 show D/T MODEM/FAX/TEL APPLICATION. Figure 10-Figure 12 show SWITCHING SYSTEM.

Figure 8. D/T MODEM/FAX/TEL APPLICATION

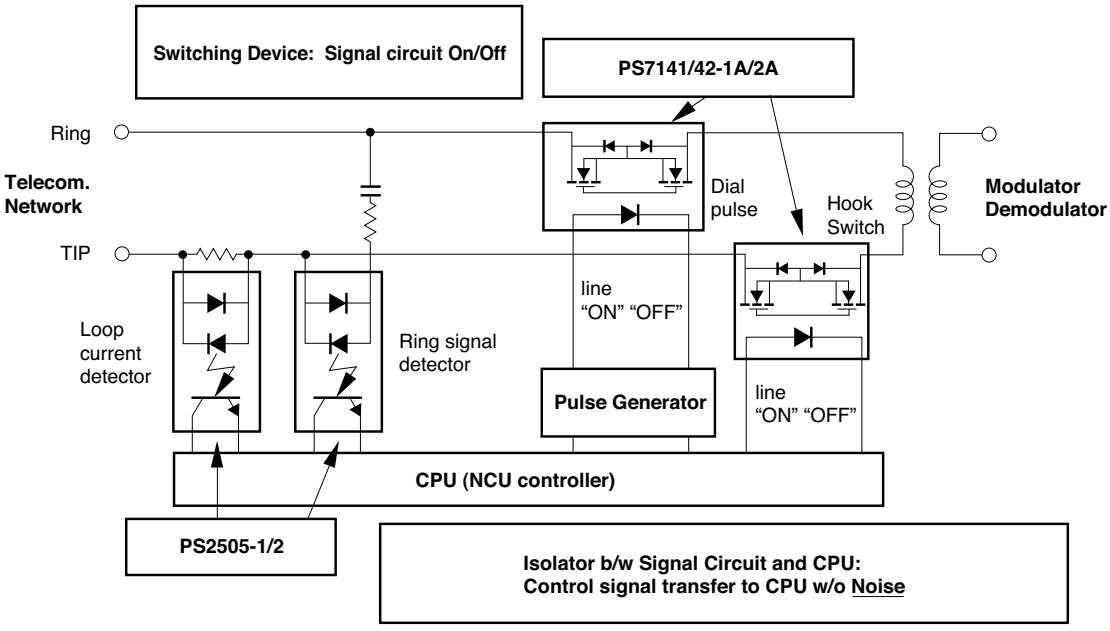


Figure 9. PC CARD/BOARD MODEM

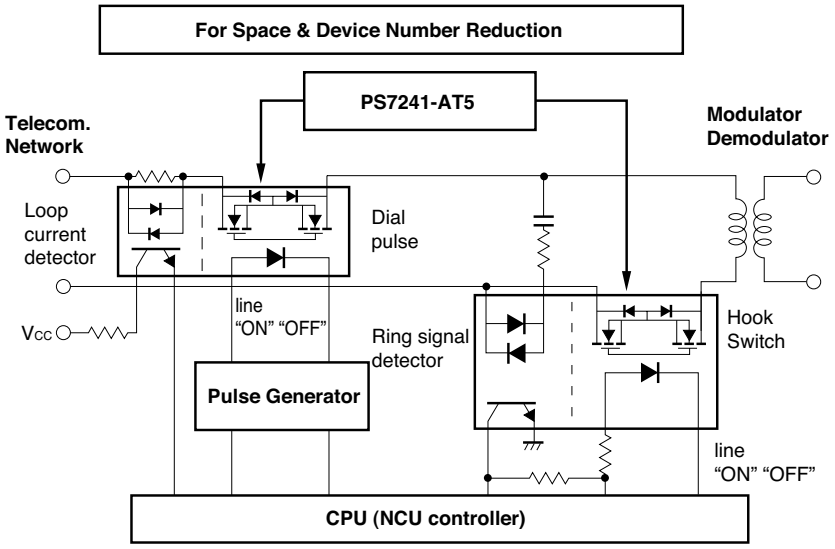


Figure 10. SWITCHING SYSTEM

Example of NRT (No Ringing Trank) signal control

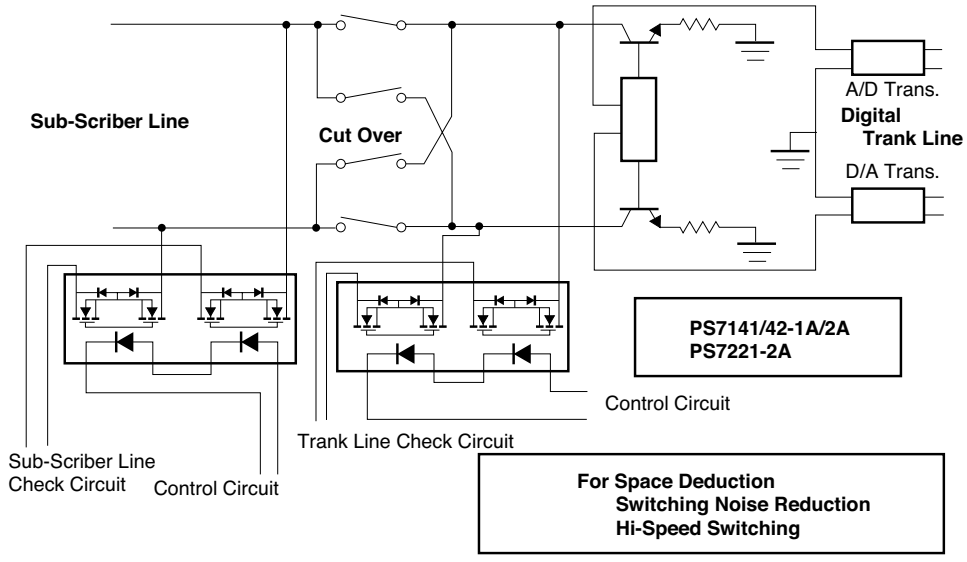


Figure 11. SLOW SWITCHING TYPE

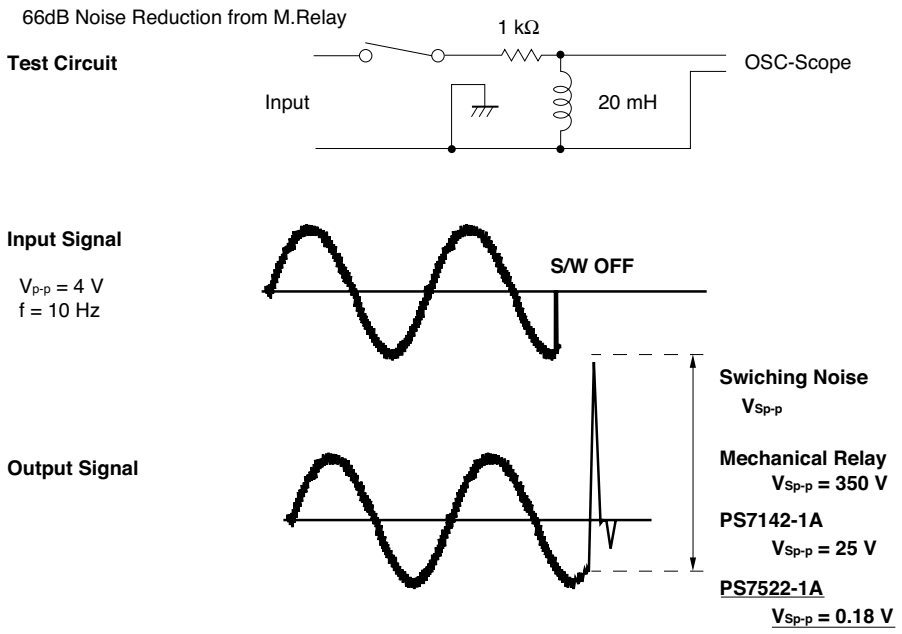
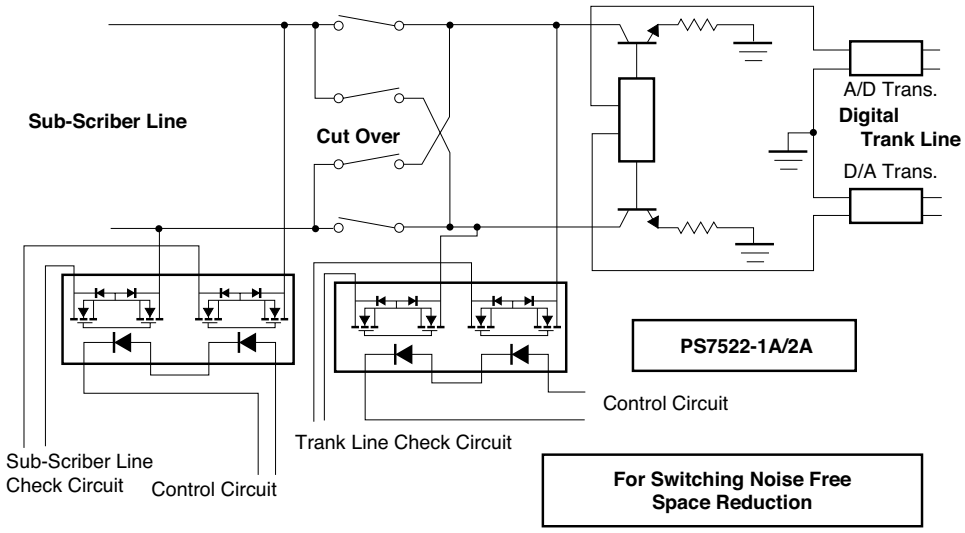


Figure 12. SWITCHING SYSTEM (LOW S/W NOISE)

Example of NRT (No Ringing Trank) signal control



5.2 INPUT/OUTPUT INTERFACE

The number of process control systems providing feedback control with microcomputers and minicomputers has been increasing rapidly in the past few years.

In these systems, it is necessary for the microcomputer to control the current for driving the actuator and process devices using a minute signal and to absorb the difference in signal levels or potentials between the devices.

Moreover, noise from the current turning on/off in the actuator or process device and from external devices may cause erroneous operation of the microcomputer. Therefore such noise must be cut off by the interface.

Accordingly, the interface relay in these system must provide electrical isolation for the circuits and input/output separation that shuts out the effect of noise produced mutually by input/output circuits and a transient load.

The opto MOS FET offers complete electrical isolation and insulation between the outputs by photo coupling. It can control signals and loads over a wide range by input of a minute amount of power. It is therefore suitable for the above purposes. Namely, it can be used in a sequence controller, programmable controller (PLC), robot, NC machine tool, automatic assembling machine, motor/solenoid/valve control.

Figure 13 and Figure 14 show PLC APPLICATION.

Figure 13. PLC (Input interface block)

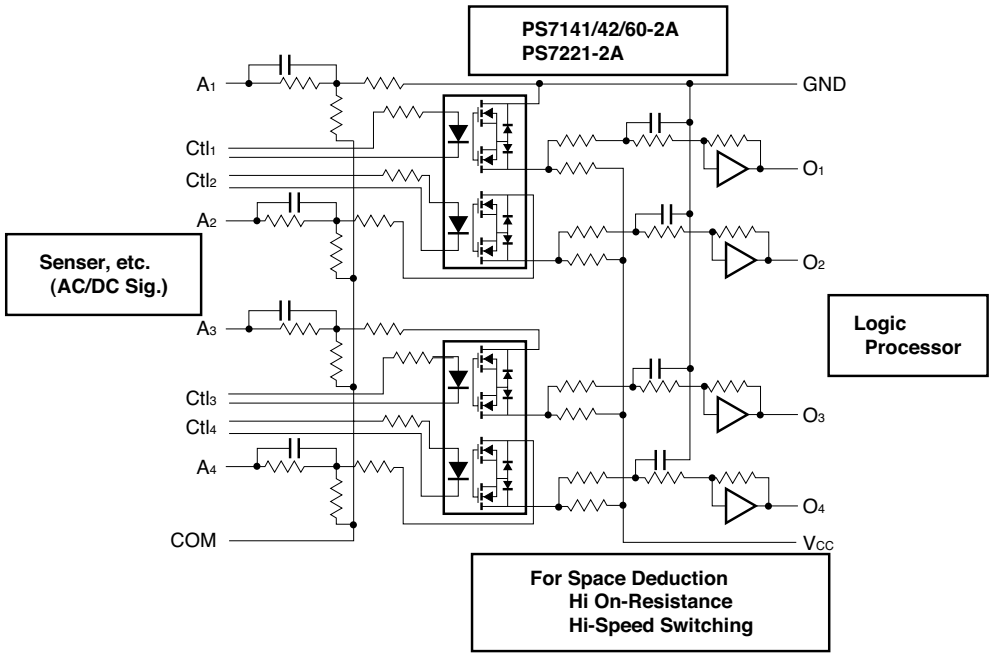
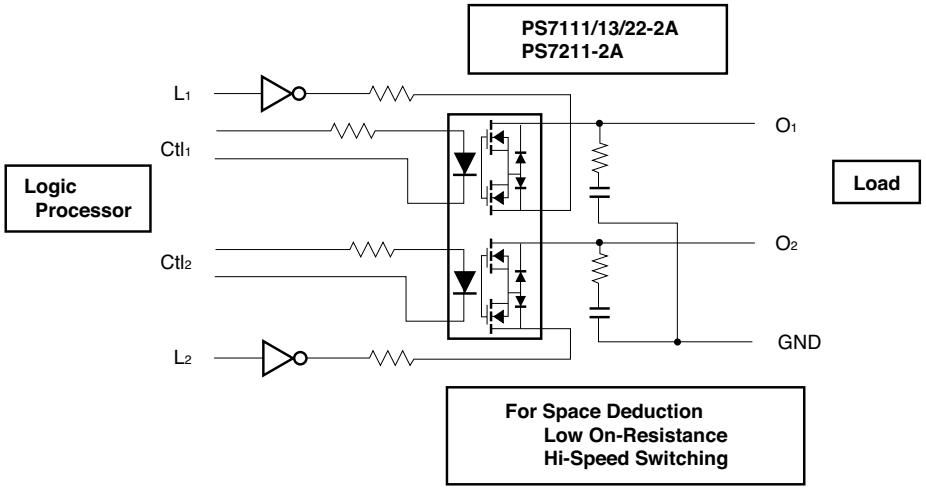


Figure 14. PLC (Output interface block)



5.3 LOW-LEVEL/ANALOG SIGNAL CONTROL

In many industrial systems, including production systems, high-speed detection of minute level signals and analog signals from sensors and transducers and transmission of these signals without distortion are frequently required for measurement, testing, inspection, monitoring, and control.

A relay to be used for these purposes must offer high-speed operation, no chattering at the time of contact, a linear characteristic without an offset voltage in the ON state, and low leak current in the OFF state.

The OCMOS FET satisfies these needs. It can be used, for example, in a collector and measuring instrument (multiplexer) for various kinds of data as well as in testing equipment (IC tester, board tester, etc.).

Figure 15 shows EQUIPMENT SYSTEM.

Figure 15. EQUIPMENT SYSTEM

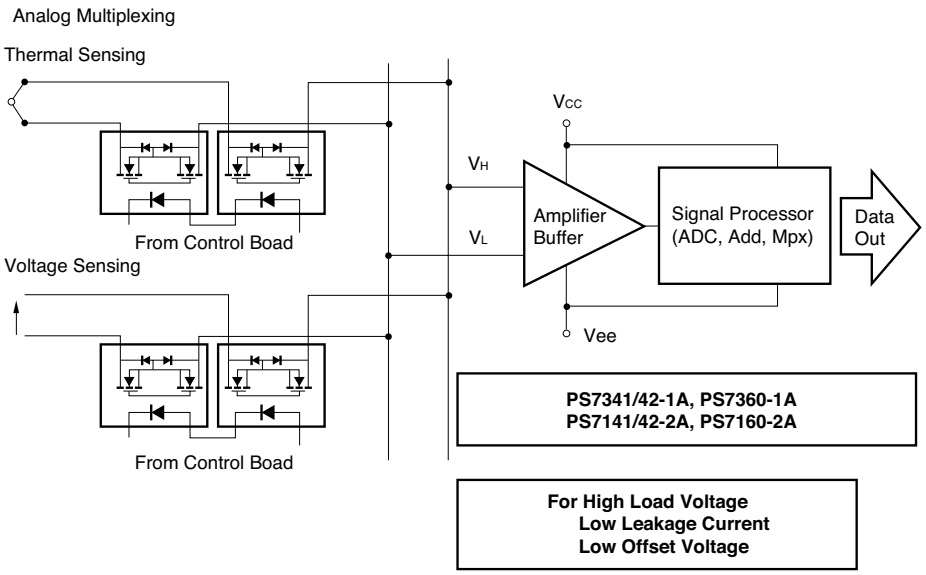


Table 5. OCMOS FET LINE-UP AND APPLICATION

Family No.		PKG	Application	Feature
2ch	PS7241-ATX	8 pin SOP	PC card, Telephone, MODEM, FAX	? 1 OCMOS FET ? 1 Photocoupler ? Small PKG
1ch	PS71XX-1A	6 pin DIP	Switching System Equipment	? Long Life ? Smaller than M. Relay
	PS73XX-1A	6 pin DIP	Equipment	? Hi-isolation b/w Ctl & Switch circuit
	PS75XX-1A	6 pin DIP	Switching System	? Slow switching (Reduction S/W Noise)
2ch	PS71XX-2A	8 pin DIP	Switching System, PLC	? Long Life ? Smaller than M. Relay
	PS72XX-2A	8 pin SOP	Switching System, PLC	? Small PKG
	PS75XX-2A	8 pin DIP	Switching System	? Slow switching (Reduction S/W Noise)

6. COMPARISON WITH OTHER SWITCHING DEVICES

Table 6 show the comparison OCMOS FET with other switching device.

Table 6. COMPARISON OF FEATURE

	OCMOS	M.Relay	Tr.P.C.	Triac P.C.
Signal Linearity	Excellent	Excellent	Fair	Poor
S/W Power	Small to Midium	Small to Large	Small	Midium to Large
Power Consumption	Excellent	Fair to Good	Excellent	Fair
Number of Operation	Excellent	Depend on S/W Po.	Excellent	Excellent
S/W Noise	Almost Nothing	Exist	Almost Nothing	Almost Nothing
t_{on}/t_{off}	Excellent	Fair	Good	Good
Mechanical Shock	Excellent	Fair	Excellent	Excellent
Package	LOW Profile SOP	Multi-ch 1 PKG SMD	SOP, SSOP	SOP

OCMOS: Opto-coupled MOS FET, M.Relay: Mechanical Relay,
Tr.P.C.: Tr.Output Photocoupler, Triac P.C.:Triac Output Photocoupler

7. CAUTIONS FOR USE

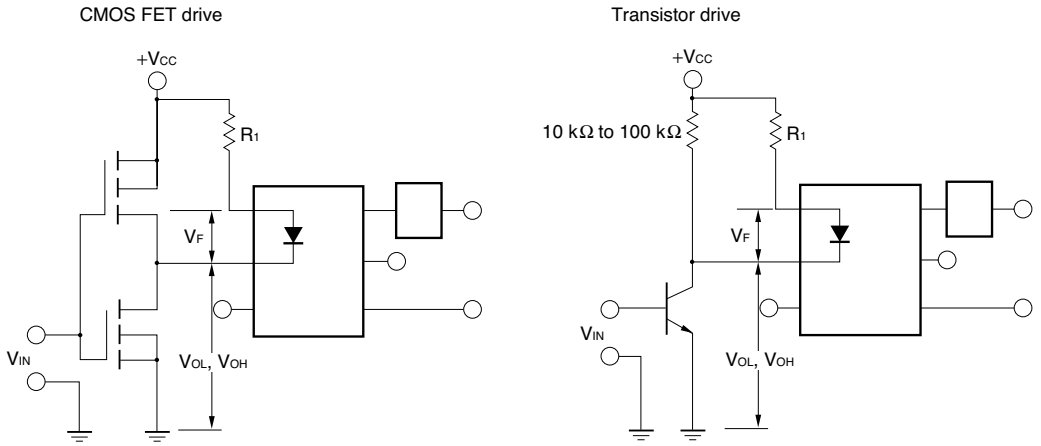
- **OCMOS FET Driving Conditions**

To assure normal turn-on and turn-off actions of the relay, use the following driving conditions:

	min.(note)	typ.	max.
Forward LED current to turn on: I_F (on)	2 mA	10 mA	20 mA
Forward LED voltage to turn off: V_F (off)	0 V	–	1 V

Note For the conditions above, the on-state resistance, load current, turn-on time, and some other parameters differ from those provided in the standard specifications.

Typical OCMOS FET Driving Circuits



How to Determine LED Current-Limiting Resistance Needed to Assure Turn-On Action:

Current limiting resistance: $R_1 = \dfrac{V_{CC} - V_{OL} - V_F\,(on)}{2 \text{ to } 20 \text{ mA}}$

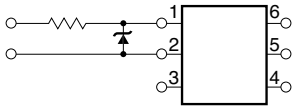
How to Determine LED Forward Voltage Needed to Assure Turn-Off Action:

Turn-off voltage (forward LED voltage): $V_F(off) = V_{CC} - V_{OH} < 1$ V

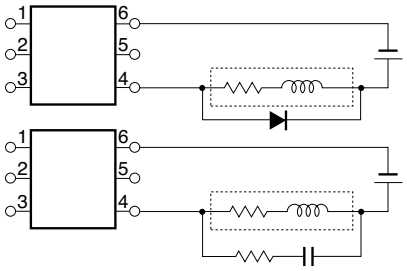
- Untimely Turn-Off Action
  A sudden drop in LED drive current can cause untimely turn-off action of the OCMOS FET when it is in on-state.
- Misoperation due to Impulsive Input Current in Off-State
  If a large, impulsive current flows into the OCMOS FET's control input when it is in off-state, the OCMOS FET may momentarily misoperate. The relay will return to off-state when the pulse current is removed, however. To prevent such misoperation, use a pulse current with the product of its peak value (IP) with pulse width (? t) not exceeding 700 ? $10^{?9}$ (ampere second).
- OCMOS FET's Electrostatic Capacity
  In the off-state, the output OCMOS FETs have a capacitance of several hundred picofarads. Note, therefore, that, if the load voltage suddenly changes, a transiental charging/ discharging current flows through the load circuit even when the OCMOS FET output is off-state.

- Note on Continuous, High-Speed Switching
  Relay's maximum response speed (frequency) depends on the input current intensity:
  e.g. 1000 Hz max. at I_F = 10 mA
  500 Hz max. at I_F = 5 mA
- Surge Protection
  If a reverse surge voltage is expected across the control inputs, use a Zener diode across the input pins to suppress surge voltages exceeding 5 V. If large spikes exceeding the device's absolute maximum ratings are expected at the output from an inductive load, use a C/R snubber or clamping diode in parallel with the load to suppress such spikes.

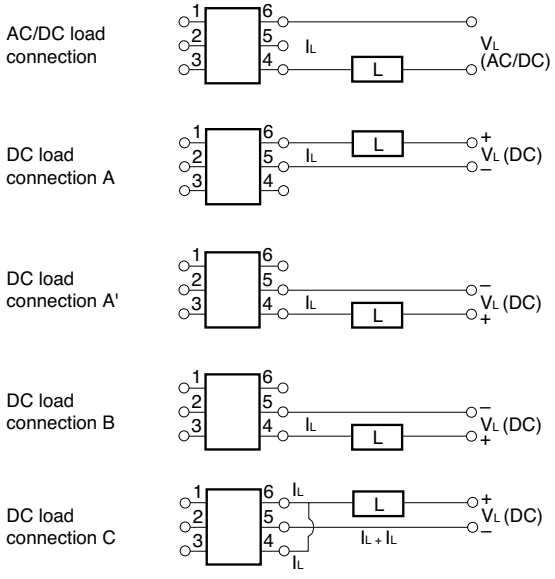
Surge Protection for Control Inputs



Spike Protections for Output Circuit



- **Load Connections**
  PS Series (AC/DC Switching Version)
  The following five types of load connections are available.
  Choose one or more depending on your application purpose.



- Input-Output Short Circuit
  If an input pin is shorted to an output pin while the OCMOS FET is active, it may cause permanent damage to the internal circuitry. Take care never to short one to the other.

- **Handling Precautions**
- Electrostatic damage to OCMOS FET
  The output OCMOS FET has a pin-to-pin electrostatic destruction voltage of 2000 V (test condition: 100 pF, 1.5k ohms). Care must be taken to protect the device from static electricity exceeding this value.
- Lead strength
  Never apply a bend stress of more than 500 grams to any lead as it may cause damage to the OCMOS FET package and mar the device's performance and/or reliability.
- Soldering
  Observe the following soldering conditions:
  Dip soldering:
  Prebake condition: 165 °C, Not longer than 60 sec.
  Soldering condition: 260 °C, Not longer than 10 sec.
  Soldering with soldering iron:
  Iron tip temperature: 280 to 300 °C
  Iron wattage: 30 to 60 watts
  Soldering duration: Not longer than 5 sec.
- Post-installation cleaning
  Observe the following cleaning requirements for OCMOS FET mounted on a PC board:

	Recommended	Not recommended
Cleaning solvent	Isopropyl alcohol Ethylalcohol	Trichloroethane Toluene Xylene

Cleaning method	Yes/No
Steam	No
Ultrasonic	Conditional yes
Brushing	No
Dipping in solvent	Yes

8. CONCLUSION

Demand for OCMOS FET featuring high sensitivity, low driving power, extremely low offset voltage in the on-state and very small leak current in the off-state is steadily increasing.

At the same time, various problems will occur in their circuit design.

We hope this manual will be helpful in solving such problems.

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